

DROPOUT VOLTAGE IS NOT THE ONLY IMPORTANT CHARACTERISTIC OF A LOW-DROPOUT REGULATOR. NOISE, RIPPLE REJECTION, AND WAKE-UP TIME CAN ALSO SIGNIFICANTLY AFFECT THE PERFORMANCE OF A LOW-NOISE, PORTABLE SYSTEM.

Get the best from your low-dropout regulator

Thanks to their weak insertion losses, low-dropout (LDO) regulators occupy a place of choice in battery-operated systems. The level of dropout used to be a designer's main concern when choosing a LDO regulator, but many LDO regulators now boast dropout numbers of 150 mV at 100 mA. Current marketing requirements, particularly for portable and low-noise applications, demand more from LDO regulators than just low dropout. Designers now want regulators with low output noise, high ripple rejection, and low quiescent current. Power-on and wake-up characteristics are also important in some applications. Obtaining the best performance from these parameters requires that you fully understand how an LDO regulator works and how these parameters affect your application.

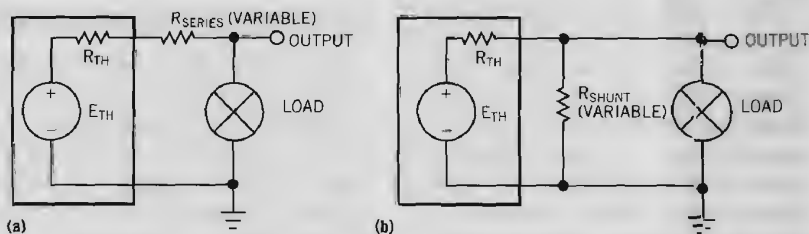
AN LDO REGULATOR IS A SERIES REGULATOR

A linear regulator always delivers an output voltage that is lower than its input voltage. The designer of an LDO regulator can implement this kind of device in several ways. The most common approach is to use a variable-resistor element that connects in series with the input source—a series regulator (Figure 1a)—or an element that connects across the load—a shunt regulator (Figure 1b). The shunt version is unpopular, except for use with current sources, such as solar arrays. Most LDO regulators use a series element.

The series element, or "ballast," must permanently sustain the difference between the input and output voltages (Fig-

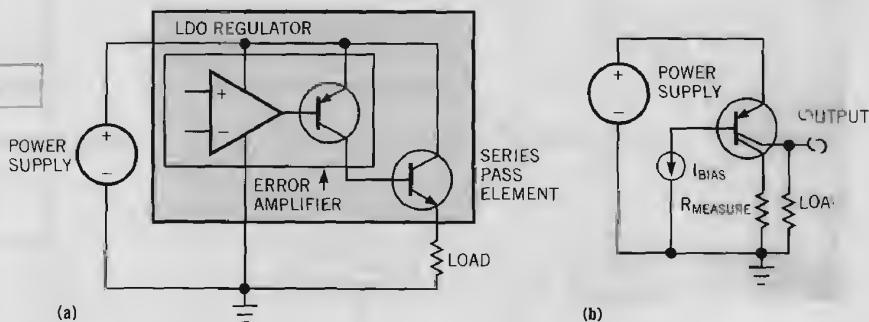
ure 1a.) Because the load current flows through this resistor, you can easily calculate the power that this resistor dissipates in heat: $P_{\text{LOSS}} = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}}$. The voltage difference $V_{\text{IN}} - V_{\text{OUT}}$ is the so-called dropping voltage, and this voltage determines the maximum power that the LDO regulator's package can safely dissipate.

Figure 1



A series regulator (a) connects the variable resistor in series with the input. A shunt regulator (b) connects the resistor across the load.

Figure 2

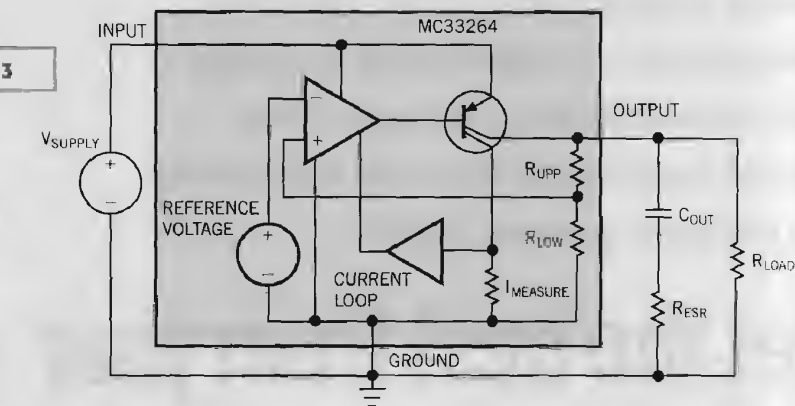


A classic bipolar regulator architecture (a) uses a pnp element to drive an npn series-pass transistor. Using a pnp transistor as the series-pass element (b) solves the floating-emitter issue.

Either a bipolar transistor or a MOSFET implements this variable resistor. A bipolar implementation consists of a classical ballast stage that surrounds an npn transistor (Figure 2a). A pnp transistor, which is the output stage of an error amplifier, drives the npn element.

The npn transistor receives its bias current from the input rail and through the pnp transistor. The emitter then evacuates this bias current to contribute to the output current. To ensure proper operation, the biasing circuit must always keep the base's potential higher than the emitter's potential. When the input-to-output differential is high, there is no problem. But if you decrease the input voltage close to the output value, the control circuit pushes the series-pass element toward saturation to ensure proper operation of the regulator, and the value of the transistor-equivalent variable resistor decreases. Unfortunately, because the transistor needs to maintain a necessary V_{BE} level, this equivalent resistor cannot decrease indefinitely. As V_{IN} drops, the LDO regulator cannot maintain the regulation, and the output voltage drops.

This configuration is similar to that of a high-side switch for which the emitter of the transistor or the source of an N-channel MOSFET requires a separate, floating power supply. You can add this supply using the bootstrap technique common to half-bridge-based applications, but it is difficult to implement this technique in a low-noise linear regulator. In Figure 2a's circuit, the minimum dif-



A simplified block diagram of a bipolar LDO regulator helps you make some simple stability observations.

ferential voltage within regulation equals $V_{CE(SAT)}(pnp) + V_{BE}(nnp)$. If $V_{CE(SAT)}(pnp)$ is 200 mV and $V_{BE}(nnp)$ is nearly 600 mV, the dropout is 800 mV, an unacceptable value for battery-operated systems. In the 78XX series of regulators, a resistive shunt provides the circuit with current protection but also contributes to the overall voltage drop.

PNP TRANSISTORS AS HIGH-SIDE SWITCHES

Because the npn transistor's emitter is floating in Figure 2a's circuit, another way to lessen the dropout voltage as the transistor approaches saturation is to reverse the bipolar transistor and secure its emitter to the supply rail. In this case, a floating supply is unnecessary, and the bias path to ground is immediate. Figure

2b, which uses a pnp transistor, shows this alternative approach. It is easier to control this circuit as it approaches saturation, because you force a higher base current simply by pulling the base closer to ground. Unlike the npn-transistor-based circuit, the dropout of Figure 2b's circuit is the pnp transistor's saturation voltage $V_{CE(SAT)}$ or a MOSFET's $R_{DS(ON)} \times I_D$. By selecting a high-gain series transistor, dropouts as low as 60 mV at 100 mA are possible. The bias current in Figure 2b flows to ground and no longer contributes to the output current. This "ground current," which data sheets specify, is a typical characteristic of bipolar LDO regulators. The value of this ground current directly depends on the series transistor's gain. After achieving a

Figure 4:

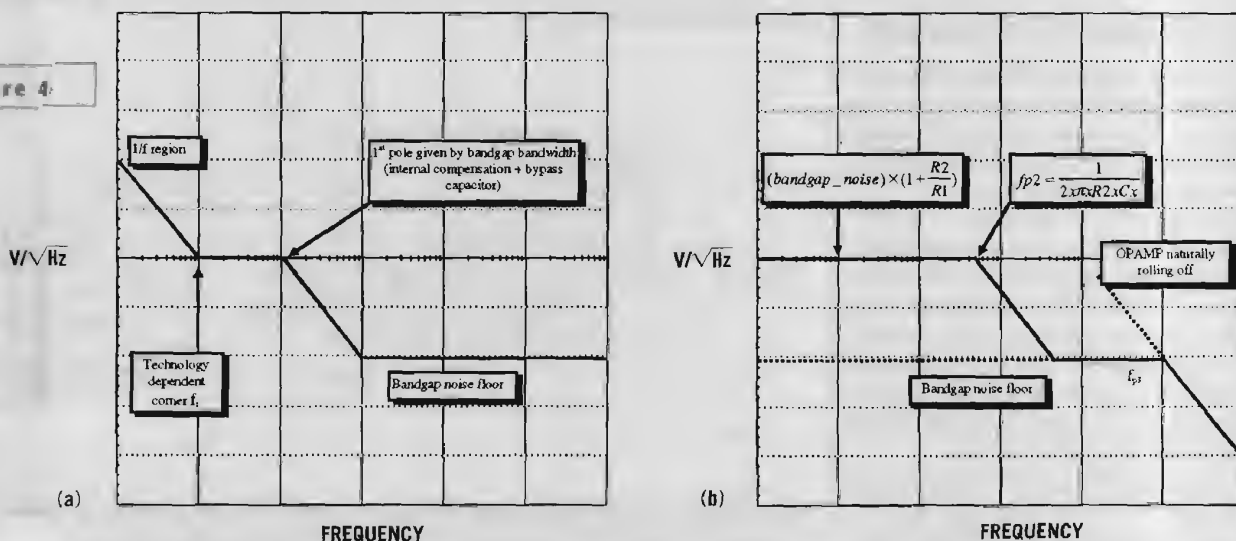
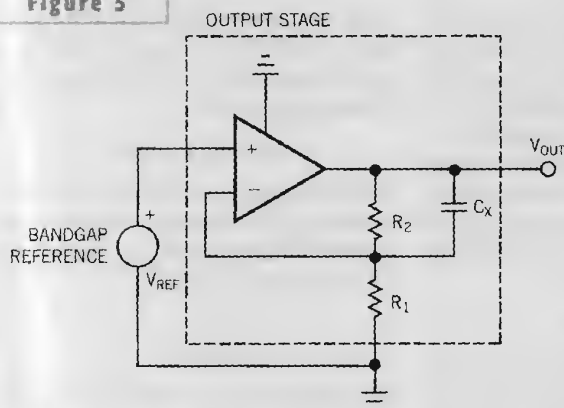


Figure 5



This simplified schematic helps determine the LDO regulator's noise spectrum. The error amplifier amplifies the bandgap noise by $1+R_2/R_1$, and C_x/R_2 add a pole at f_{p2} to tailor this gain.

small dropping voltage, it would be a pity to degrade this voltage by using a shunt element. For that purpose, a multicollector transistor provides the necessary cells to sense a fraction of the output current and feed it back to a protection loop.

Most LDO regulators consist of a bandgap reference and an error amplifier whose output stage integrates the series-pass pnp transistor. Figure 3 shows a simplified diagram of a bipolar LDO regulator. You can view the series-pass element as a transconductance generator with transconductance $g_m = I_{DQ} / \partial V_{BE}$. In this case, you can derive the following transfer function, excluding the error amplifier, from Figure 3:

$$\frac{V_{OUT}}{V_{PIN+}} = \frac{g_m \times R_{LOAD} \times (1 + sZ_1)}{1 + sP_1} \times \left(\frac{R_{UPP}}{R_{UPP} + R_{LOW}} \right)$$

You can use this equation, where $Z_1 = R_{ESR} \times C_{OUT}$, and $P_1 = (R_{LOAD} + R_{ESR}) \times C_{OUT}$, to perform a simple stability analysis and to study how the poles and zeros affect the noise. As you can see from the transfer equation, no inherent pole exists except the one that the output capacitor produces. Without this capacitor, there would be no element to roll off the gain to 0 dB at reasonable frequencies; thus, the regulator's stability in the upper portion of the spectrum would be in jeopardy. The capacitor's ESR value is also important. Some ESR can improve system stability, but too much ESR can degrade it. Motorola always specifies an ESR range in which the regulator is stable. A well-designed regulator accepts ESR between a few 10s of milliohms and 5Ω. Complete regulator designs

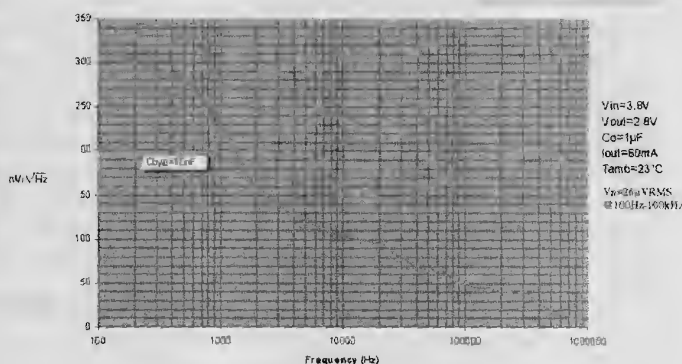
include complex compensation networks at strategic places to ensure the device stays stable regardless of the load.

BIPOLAR TECHNOLOGY BOASTS LOW NOISE

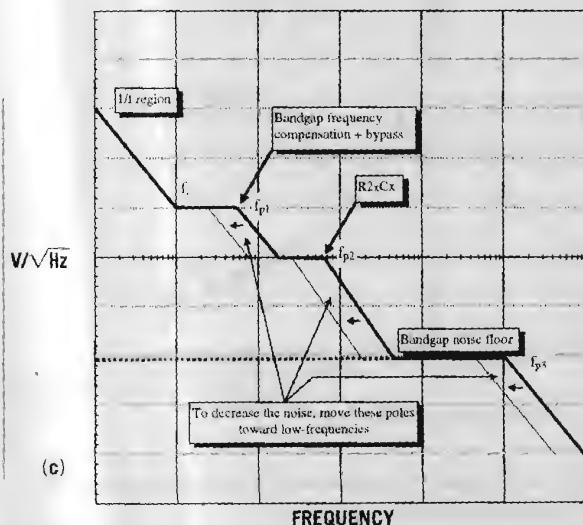
To study noise effects, split an LDO regulator into two blocks: a bandgap reference and an error amplifier/output stage. The dc noise characteristics of each stage are the main contributors to the LDO regulator's noise. However, the ac behavior of the regulator's compensation stages also impacts the global performance.

For a power supply of a noise-sensitive circuit, such as an RF VCO, the noise superimposed on the supply line is a key contributor to the overall noise floor. Several types of noise exist (Reference 1). Johnson, or white, noise comes from the thermal agitation of electrons in resistive portions of the circuit, such as a transistor's base and bias resistors. The power spectrum of this type of noise is flat until a certain frequency cutoff. In other words, each harmonic theoretically transports an equal level of energy over the spectrum under consideration. Flicker, or "1/f," noise, depends on the quality of the process and exhibits a 1/f envelope. This "pink" noise transports the same level of energy integrated over each decade of frequency. Shot noise describes the fluctuations of a current flowing in a junction around its steady-state value. Shot noise also produces a flat power spectrum; it is a type of white noise. In the low-frequency range of the LDO regulator's noise, 1/f noise prevails until you reach a technology-dependent frequency

Figure 6



Noise-density plots provide insight on the noise performance of an LDO regulator, such as the MC33263, which has low-noise performance tailored to telecommunications applications.



The noise spectrum of a typical bandgap reference (a) shows the initial 1/f slope, the corner at f_c , and the effect of the bandgap reference's bandwidth pole. The noise spectrum of a typical output stage (b) shows additional poles at f_{p2} and f_{p3} . Combining these two graphs (c) reveals the overall noise behavior of the LDO regulator.

corner, f_c , at which point white noise predominates.

Figure 4a describes a typical noise spectrum of a bandgap reference. The noise decreases with a 1/f slope until you reach f_c . The bandgap reference's bandwidth adds a pole, f_p . The designer of the LDO regulator internally fixes the location of this pole; you can change the location using an external bypass capacitor. If the bypass capacitor's value is high, this capacitor rolls off the bandwidth and accordingly dwindles the noise. The most important part of the noise spectrum is the bandgap noise floor.

Now, consider the noise of the output stage. **Figure 5** shows a simple connection of the reference voltage to the output stage. In this case, the error amplifier is in a noninverting configuration with a gain of $1+R_2/R_1$, which affects the bandgap noise. Because an LDO regulator is a low-frequency device, gain is unnecessary in the upper portion of the spectrum. C_x and R_2 introduce a second pole at f_{p2} to tailor the gain. When C_x shorts R_2 , the output stage acts as a simple follower. The error amplifier adds a third pole, f_{p3} . **Figure 4b** shows the output stage's noise spectrum, and **Figure 4c** combines the bandgap and output stage's noise spectrums into one graph.

Analyzing this noise curve provides you with some clues about which of the following options you may be able to use to reduce the total rms noise:

- Decrease the frequency of f_c . Unfortunately, this change is impossible because the silicon material dictates the value of f_c .
- Diminish the bandgap reference's noise floor. However, the user doesn't have direct control over this parameter. Instead, the designer of the regulator keeps the noise level low by using good design rules and clever transistor architecture and selection and by assuring low base resistance and sufficiently high collector current for critical transistors in both the bandgap reference and the output stage (Reference 2).
- Roll off the bandgap reference's bandwidth by internal frequency compensation or via the bypass capacitor.
- Move f_{p2} toward low frequencies by increasing the $C_x \times R_2$ time constant.

Unfortunately, high values of R_2 increase the thermal noise, and larger values of C_x require more die area. In common designs, decreasing f_{p2} below several 10s of kHz is difficult.

- Use low-bandwidth op amps when noise density higher than 500 kHz is critical. When the noise target stays within 100 kHz, low-bandwidth op amps are unnecessary.

WATCH OUT FOR NOISE SPECS

The power or the energy content of white noise is equally distributed over the spectrum of interest. Theoretically, if you measure at any frequency with a power meter, you always find the same value. If the noise is not white or is a mixture of white and 1/f components, its power content is no longer equally distributed over the spectrum. You then must define a bandwidth, B, in which you measure noise power. The noise power becomes a

power noise density expressed in watts per hertz. You can evaluate power as a mean square value (msv) using the following formula:

$$\text{msv} = \frac{1}{T} \int_0^T [f(t)]^2 dt.$$

If you relate the msv to the energy of each harmonic, you can also express the power as the following equation, where C_n are the Fourier coefficients:

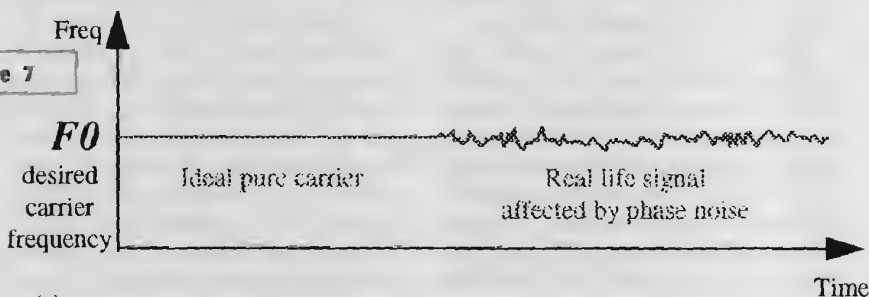
$$\sum_{n=-\infty}^{\infty} |C_n|^2.$$

Extract the square root of the msv to obtain the rms voltage:

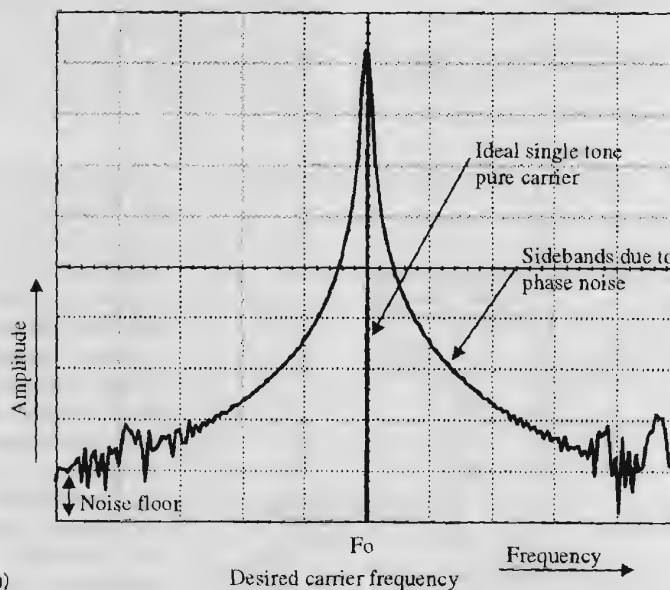
$$\sqrt{W/\text{Hz}} \Rightarrow V_{\text{RMS}}/\sqrt{\text{Hz}}.$$

This explanation demonstrates three important points. First, because the power density of an LDO regulator is not equally distributed over the spectrum of interest, expressing an LDO regulator's power density without a frequency ref-

Figure 7



(a)



(b)

Oscillator-induced noise modulation causes a carrier to move around its nominal frequency, which you can view in the time (a) and frequency (b) domains.

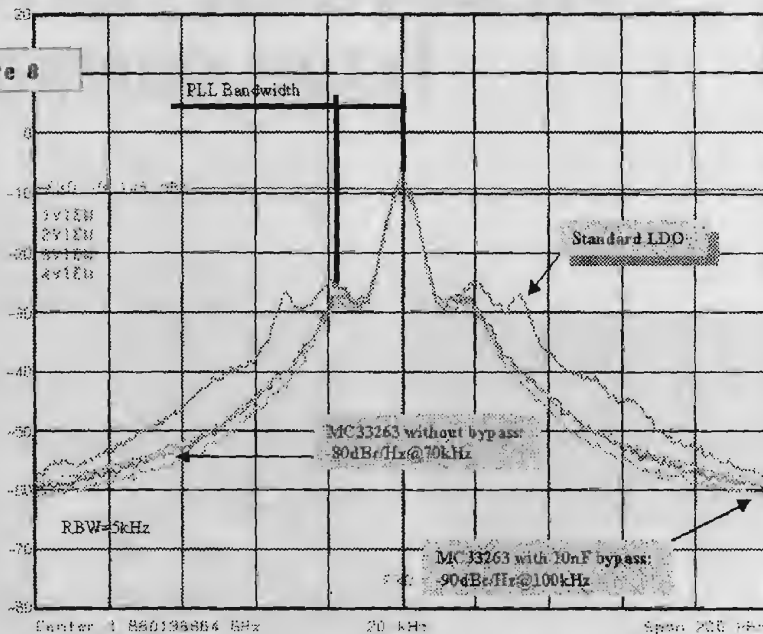
erence is nonsense. An example of a complete power-density specification should read "200 nV/ $\sqrt{\text{Hz}}$ at 1 kHz." Second, any total rms noise-level specification that lacks bandwidth information and minimum operating conditions inaccurately indicates the noise level. This point is particularly important for narrow bandwidths. An adequate specification is $100 \mu\text{V}_{\text{RMS}} < 100 \text{ Hz}$ to 1 MHz at $I_{\text{OUT}} = 50 \text{ mA}$. Third, plots of spectral-noise-density versus frequency assess the noise of an LDO regulator. The noise-density level over a particular operating spectrum that extends between the PLL's bandwidth is important to a designer. If the noise component is inside the PLL bandwidth, the PLL will have sufficient gain to fight it. However, if the noise is out of the bandwidth, the PLL can't get rid of it, and you see the noise on the output. Neither a simple amplitude-versus-frequency plot nor a total rms level—for which integration smoothes ungraceful peaks or resonances—gives you much insight. Motorola provides spectral-density plots to clearly show an LDO regulator's noise performance (Figure 6).

LDO AFFECTS VCO's PERFORMANCE

A VCO and associated loop circuitry is critical to a radio. The VCO block's overall behavior and, specifically, its noise performance affect the radio's most important specifications: spectral purity of the transmitter, selectivity of the receiver, noise and hum in analog transceivers, and phase error in digital systems. Some designers use the VCO's extreme sensitivity to external perturbations to design low-cost regenerative and super-regenerative receivers. Although a comprehensive review of the theory of oscillator noise would require an entire book, a short review demonstrates how an LDO regulator's noise impacts a VCO's performance and how noise can plague a radio design.

Noise can affect oscillator phase and amplitude characteristics. You can—with some simplifications—consider pure phase noise as phase or frequency modulation of a carrier by a random signal. Figure 7a depicts how the carrier moves around its nominal

Figure 8



LDO regulators have different effects on a PLL's behavior because of the regulators' differing noise qualities.

frequency because of noise modulation. Figure 7b shows the same phase noise in the frequency domain. Without phase noise, this spectrum would consist of a single ray at the nominal frequency. With phase noise, sidebands appear.

AN LDO, A VCO, AND NOISE

A VCO is the seat of thermal, flicker, varactor, and pushing phase-noise sources. The oscillator loop amplifies thermal noise, which consequently modulates the carrier. Linear approaches to studying this type of noise are common and lead to such equations as Leeson's model (Reference 3). Flicker noise depends on active elements and even pas-

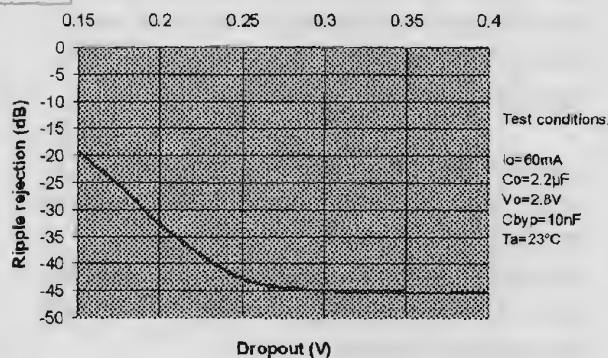
sive components. Analyzing this noise usually requires nonlinear approaches. Nevertheless, simple models, such as the enhanced Leeson's model (Reference 4) or others, are still suitable. This enhanced model reveals $1/f$, $1/f^2$, and $1/f^3$ noise terms. It also shows the tremendous impact of the resonator's loaded Q on the feedback loop and the impact of the output power on the flicker noise number.

For our discussion, varactor noise and pushing noise are the most significant noise sources. The design of VCOs in large-volume portable products, such as cellular and cordless phones, requires that you make trade-offs to reach your cost target. A common trade-off occurs in the tuning portion, for which high-gain tuning slopes of 100 MHz/V are common. This large gain allows a 0 to 1V control voltage and avoids the use of a costly dc/dc converter to elevate the battery voltage to 10V. Unfortunately, large gain also results in a high sensitivity to external noise.

You can consider the varactor diode as an equivalent resistor, R, usually of a few 10s of kilohms, that generates thermal noise. Without proper optimization, this diode's

Figure 9

Ripple rejection @100kHz versus dropout



At very low dropout levels, the ripple rejection at 100 kHz degrades.

external bias resistance also influences the noise if you improperly optimize it. You can express the single-sideband (SSB) noise, N , generated at an offset, f_m , from the carrier, in decibels referred to carrier or decibels below carrier, according to the following equation. K_O is the VCO gain in hertz per volts, K is the Boltzmann's constant, and T_O is the temperature in Kelvins (Reference 5):

$$N(f_m) = 20 \log_{10} \left[\frac{K_O \sqrt{4 \times K \times T_O \times R}}{\sqrt{2} \times f_m} \right]$$

For example, assume that $R=10 \text{ k}\Omega$, $f_m=100 \text{ kHz}$, and $K_O=20 \text{ MHz/V}$. Then $N(100 \text{ kHz})=-115 \text{ dBc/Hz}$. This value is not negligible in Global System for Mobile Communications (GSM) applications, for instance. For this reason, keep the tuning range as small as possible.

A noisy supply voltage easily induces amplitude noise on the VCO output. However, a noisy supply does not cause a big problem because downstream

buffers and mixers further limit the output signal. The trouble occurs in converting this amplitude modulation into phase noise—the “pushing” effect. If P is the pushing gain of the VCO (in hertz divided by volts) and Sf_m is the supply's voltage noise at f_o (in nanovolts per hertz) (measured at an offset of $f_m \text{ Hz}$ from the carrier), you can evaluate the generated frequency ripple according to the following formula:

$$\Delta f_{\text{rms}} = P \times Sf_m$$

You can also relate the ripple to a peak phase-noise deviation in radians for a 1-Hz bandwidth:

$$\theta_{f_m} = \frac{\sqrt{2} \times P \times Sf_m}{f_m}$$

Finally, you can calculate the phase noise at an offset, f_m , from the carrier:

$$N(f_m) = 20 \log_{10} \left(\frac{P \times Sf_m}{\sqrt{2} \times f_m} \right)$$

You could try to reduce the supply noise by additional filtering using RC

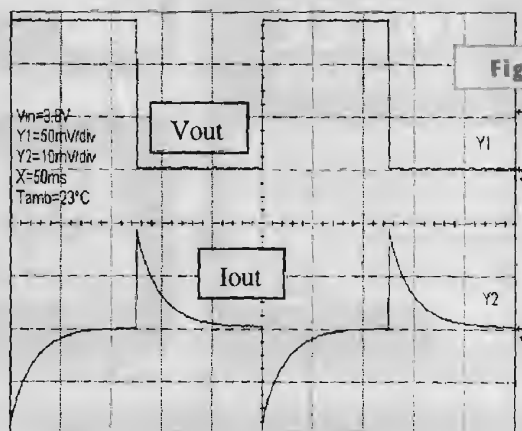
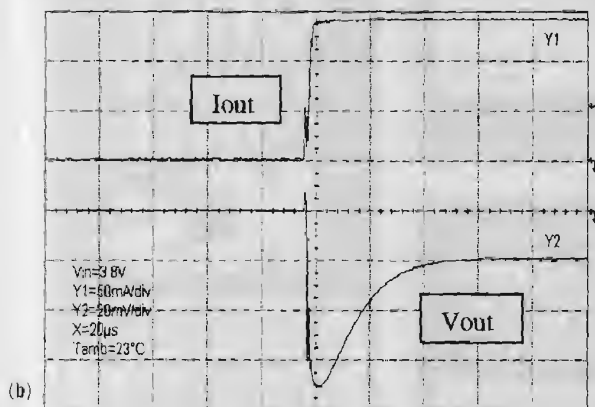
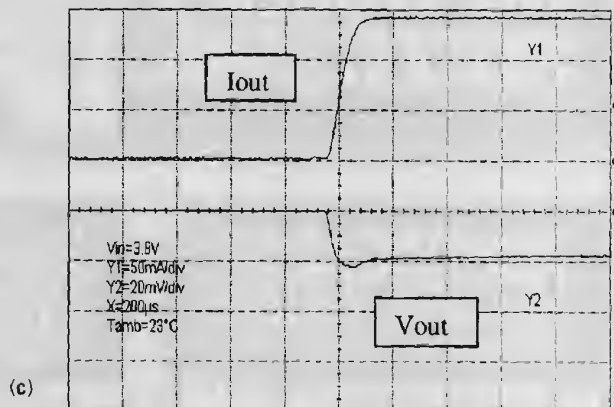


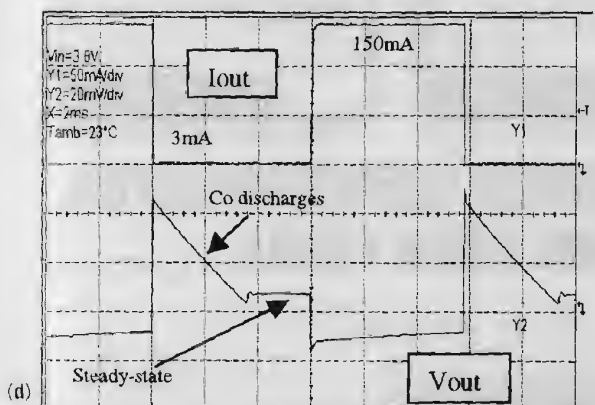
Figure 10



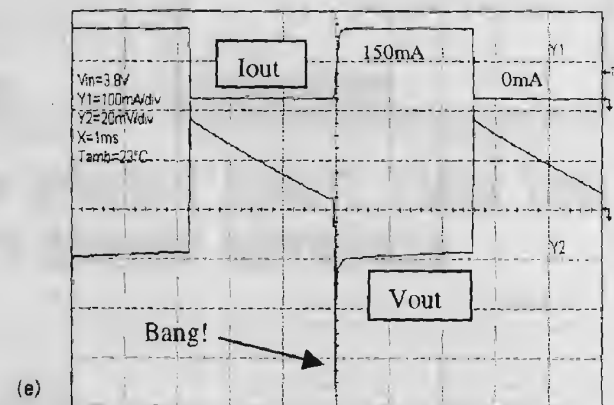
(b)



(c)



(d)



(e)

An LDO regulator's transient response takes many shapes, depending on numerous conditions: a classic transient-response waveform (a), the reaction to a current slope of $100 \text{ mA}/\mu\text{sec}$ (b), the reaction to a current slope of $2 \text{ mA}/\mu\text{sec}$ (c), transient response without any rest current (d), and the resulting response if you refire the regulator during discharge time (e), which produces a pronounced negative overshoot.

networks, but you would degrade the overall dropout of the device, and the turn-on speed would suffer from this RC integration. The only solution is to use ultra-low-noise LDO regulators.

INFLUENCE OF THE SUPPLY ON PLLs

You can attribute the noise within the PLL bandwidth—with some simplifications—to the product of the division ratio and the time reference, which is usually clean. This noise level cannot drop lower than the minimum noise floor imposed by surrounding noisy circuits, such as switching charge pumps. Outside the loop bandwidth, illustrated by a transition zone, the free-running VCO noise or the short-term VCO drift is always predominant. A spectrum analysis that uses LDO regulators with differing noise characteristics as the supply to a digital-enhanced-cordless telecommunication (DECT) synthesizer clearly demonstrates this fact (**Figure 8**).

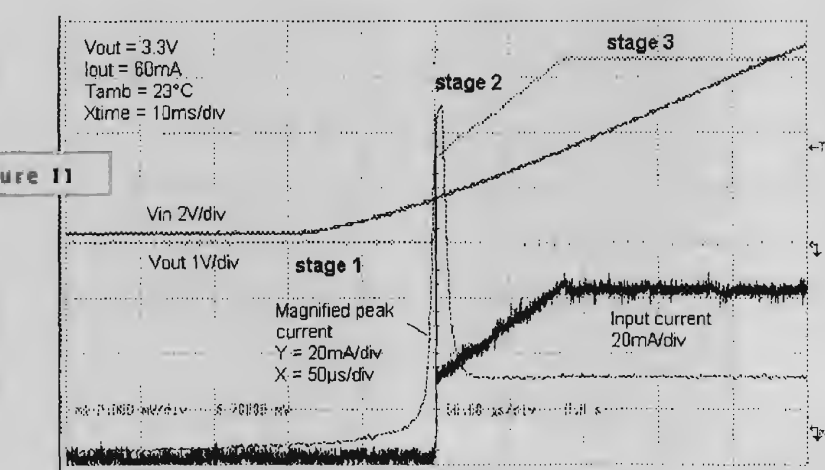
The VCO in these measurements has a pushing gain of 40 MHz/V associated with a tuning gain of 80 MHz/V. If you select an equivalent diode resistance of 10 k Ω and a noise density of 50 nV/ $\sqrt{\text{Hz}}$ at 100 kHz (the specification for the MC33263 regulator), the dc-supply and varactor noise at 100 kHz from the carrier contribute -95 and -103 dBc/Hz, respectively. Thus, the total phase noise is -92 dBc/Hz at 100 kHz or -55 dBc/Hz within a 5-kHz window of study. This number agrees with the -53 dBc/Hz observed on **Figure 8**'s plot.

A loaded-Q and flicker-noise calculation using the enhanced Leeson's model indicates an even lower and, thus, negligible LDO-regulator noise contribution. For cellular or cordless systems, pay attention to the quality of the VCO's supply and carefully select a regulator optimized for a low-noise application.

DROPOUT AND RIPPLE REJECTION

Although noise performance is critical for some systems, you still need to focus on other parameters, such as ripple rejection and the quality of the LDO regulator's response time. Ripple rejection is an important parameter for battery-operated systems. If the regulator excels in ripple rejection, it offers the downstream electronics a natural shield against choppy dc rails.

As for the output impedance, open-loop gain influences the audio suscepti-



Typical LDO start-up curves show three distinct stages and a current glitch at the onset of Stage 2 as the regulator becomes active.

bility (AS), or line ripple rejection, according to $AS_{CL} = AS_{OL} / (1 + A_{OL})$, where AS_{CL} is the closed-loop audio susceptibility, AS_{OL} is the open-loop audio susceptibility, and A_{OL} is the open-loop gain. This equation explains the good behavior of regulators in the lower portion of the spectrum and the poor behavior when they operate at higher frequencies.

Another parameter that users rarely take into account is the value of the dropping voltage that vendors use during this ripple measurement. As mentioned, the series-pass element works as a variable resistor. When the differential voltage $V_{IN} - V_{OUT}$ is high, the transistor equivalent resistor is large. The regulator has little difficulty isolating the output from the input perturbations; thus, the ripple rejection is high. If you decrease the dropout, you move the transistor operating point toward low V_{CE} s at a higher base current, at which point you may seriously degrade the conductance, g_m . The LDO regulator no longer maintains the required ripple rejection (**Figure 9**). When performing these measurements, you must avoid any input-to-output parasitic couplings—for instance, via the differential voltmeter.

DON'T SLIP ON THE SLOPE

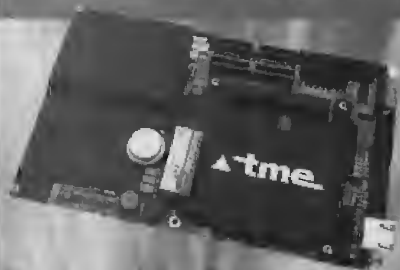
The quality of an LDO regulator's response time relates to many parameters. Among these parameters, the closed-loop bandwidth and corresponding phase margin play an important role. However, other characteristics, such as the series-pass transistor's saturation, also come into play. When a current perturbation,

such as a load increase, suddenly appears on the output, the error amplifier reacts and actively biases the pnp transistor. During this reaction, the regulator operates open loop, and the output impedance is high. The voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place. **Figure 10a** depicts the classical transient-response waveform.

The slope of the output excitation is a key parameter when specifying the LDO transient response. The steeper the slope, the richer the harmonic content of the pulse. A rich harmonic content means that frequencies much higher than the LDO regulator's bandwidth exist. The LDO regulator cannot combat the corresponding aggression, and a negative, well-pronounced undershoot occurs. To cure this problem, you need to act on your final load to brake the establishment of the current. **Figures 10b** and **10c** show the results for high- and low-current slopes, respectively.

In **Figure 10d**, the current pulses from 3 to 150 mA. This situation is comfortable for LDO regulators. Suddenly removing the load produces a positive overshoot. Thanks to the 3-mA current, a discharge path exists for the output capacitor. This path allows the internal circuit to immediately return to its steady-state level with a slightly biased series-pass element. The regulator is ready for the next shot, and the negative undershoot stays within the specs. If you pulse the output from 150 mA to zero,

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designfeature *Low-dropout regulators*

the discharge path no longer exists except through the internal feedback network. The resulting discharge is long. Unfortunately, if you bang the output during this discharge time, the negative undershoot deepens (Figure 10e). In the discharge phase, the output level is higher than the nominal value, and the circuit is asleep. The regulator pushes the error amplifier's output to its upper level to block the pnp transistor. This situation dramatically

lengthens the response to a perturbation and produces an exaggerated undershoot. Reducing the frequency of the output perturbation allows some time to recover and avoids the negative undershoot (Figure 10d).

CONSIDER THE POWER-ON PHASE

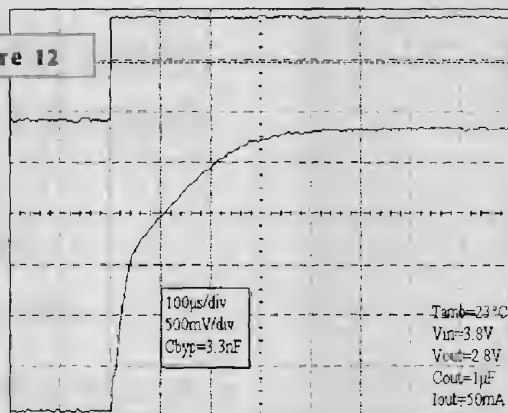
When the voltage starts to rise at the input, the regulator crosses several stages. At the beginning, when V_{IN} is low, the regulator is off and delivers no power to the load (Stage 1). When the LDO activates, it becomes a voltage follower, and its output copies the input (Stage 2). Finally, V_{OUT} reaches its nominal value (Stage 3). Figure 11 depicts this typical behavior for the Motorola MC33263. A current glitch takes place just when the regulator enters Stage 2. This glitch occurs because suddenly applying the voltage slope to the output capacitor creates a current peak ($C \times \text{div}/\text{dt}$).

WAKE UP THE LDO REGULATOR

You can use an external bypass capacitor to roll off the bandgap reference's gain and thereby reduce noise. When the LDO regulator is in shutdown mode, the bandgap is cut, and the bypass capacitor is discharged. A wake-up signal from the logic-control circuitry enables the band gap circuit, and the bypass capacitor charges toward its nominal voltage. This action slows the settling of the voltage reference and of the output voltage. Figure 12 details the typical start-up phase of the low-noise MC33263.

Waking up an LDO regulator in a short time is important in portable handset applications, in which the device routinely checks for the presence of an incoming

Figure 12



The start-up phase of an LDO regulator depends on the value of the bypass capacitor.

call. The VCO in GSM phones regularly switches on and off for this purpose. If you remove the bypass capacitor on the MC33263, the LDO reacts in less than 30 μsec , but its output noise reaches 65 μV_{RMS} over 100 Hz to 100 kHz. □

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